Project Name:

SHIMMER - Sensing Health with Intelligence, Modularity, Mobility, and Experimental Reusability

Hardware Guide

Department: DHeG Cambridge

SHIMMER Rev 1.0

Prepared By

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Version Control

Version	Date	Author	Change Description
1.0	8/10/06	B. Kuris	Document created
1.1	8/29/06	B. Kuris	MSP 6.6 and 6.7 were swapped, added mechanical drawings, added copyright notice
1.2	9/21/06	B. Kuris	Added sections on known expansions.
1.3	10/3/06	B. Kuris	Misc. Revisions. Removed Intel proprietary information

1 Purpose

SHIMMER is the code name for a small sensor platform well suited to wearable applications. The integrated 3-axis accelerometer, large storage, and low-power standards based communication capabilities allow for standalone application as a robust motion capture device for people and equipment. SHIMMER can also stream data to more-capable devices to expand the scope of annotations.

The goal of SHIMMER is to provide an extremely compact extensible platform for long-term wearable or wireless sensing in both connected and disconnected settings using proven system building blocks. The design is realized using conventional design and assembly technology to ensure repeatability and economy.

2 Capabilities Overview

Feature	Purpose	Component/Cabilities
I/O	Capture of sensor and user data	**Integrated** • 3 Axis Accelerometer using Freescale MMA7260Q 1.5/2/4/6g Micropower MEMs Accelerometer into CPU A/D • 4 Colored Status LEDs • Reset button **Expansion** • Hirose ST60 series 18 position rugged mobile style external Header for charging, programming, and tethered sensor extensions (12 multi-purpose I/O connections). • Hirose DF12 series 20 position internal Expansion Header for internal sensor daughter boards (14 multi-purpose I/O connections)
Processing	Control operating state Provide best Signal quality Operational alerts and messages	**MSP430F1611 CPU** ▪ 10Kbyte RAM, 48Kbyte Flash ▪ Up to 8MHz ▪ 8 Channels of 12bit A/D ▪ Extremely low power during periods of inactivity ▪ Proven solution in medical sensing applications
Storage	No loss of data while mobile, during network outages or while changing batteries	**MicroSD slot** ▪ Up to 2GByte currently available ▪ NAND Flash based, ~20mA read/write power
Communication	Hi-reliability Standards Based Mobility	**802.15.4 Radio** ▪ Chipcon CC2420 ▪ GigaAnt Rufa 4.1dBi Antenna **Class 2 Bluetooth™ Radio** ▪ Mitsumi WML-C46N CSR based design
Form factor	Wearable	▪ Minimum Sensor volume is 1.75” x .8” x .5” and 10 grams without Bluetooth. Comparable to a lipstick ▪ Initial durable enclosure is roughly the size of “Zippo” lighter and has provisions for expansion board and Bluetooth. The enclosure can be mounted in an MP3 player armband accessory.
Operating Life and Power	Long operating life Easy maintenance and deployment	▪ Design target is 10 days while sampling 6 channels at 50Hz w/250mAH battery. ▪ “Deep Sleep” shelf life is >1 year per battery spec ▪ Integrated Li-ion battery charger ▪ Ability to monitor and indicate power status

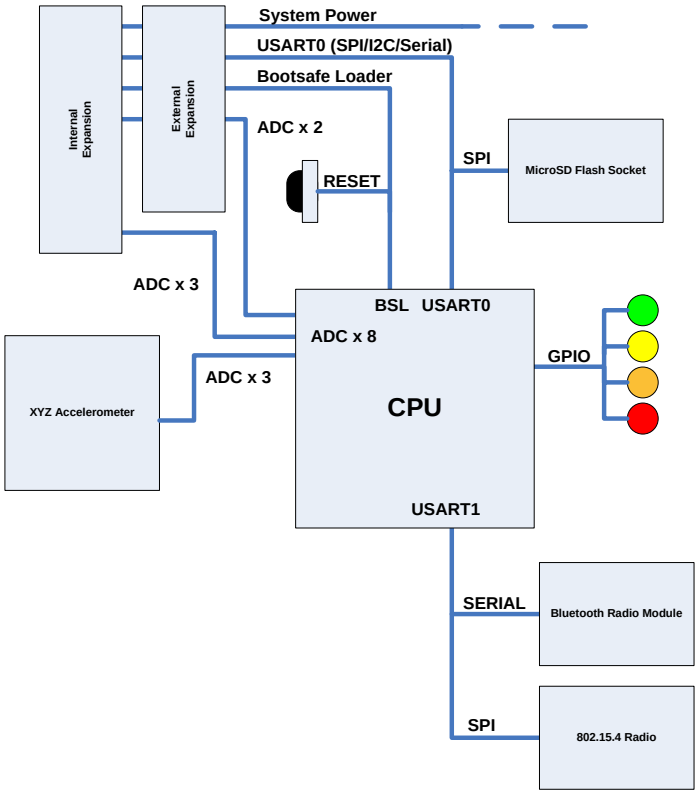


Figure 1. SHIMMER System Interconnections

3 Embedded Programming Description

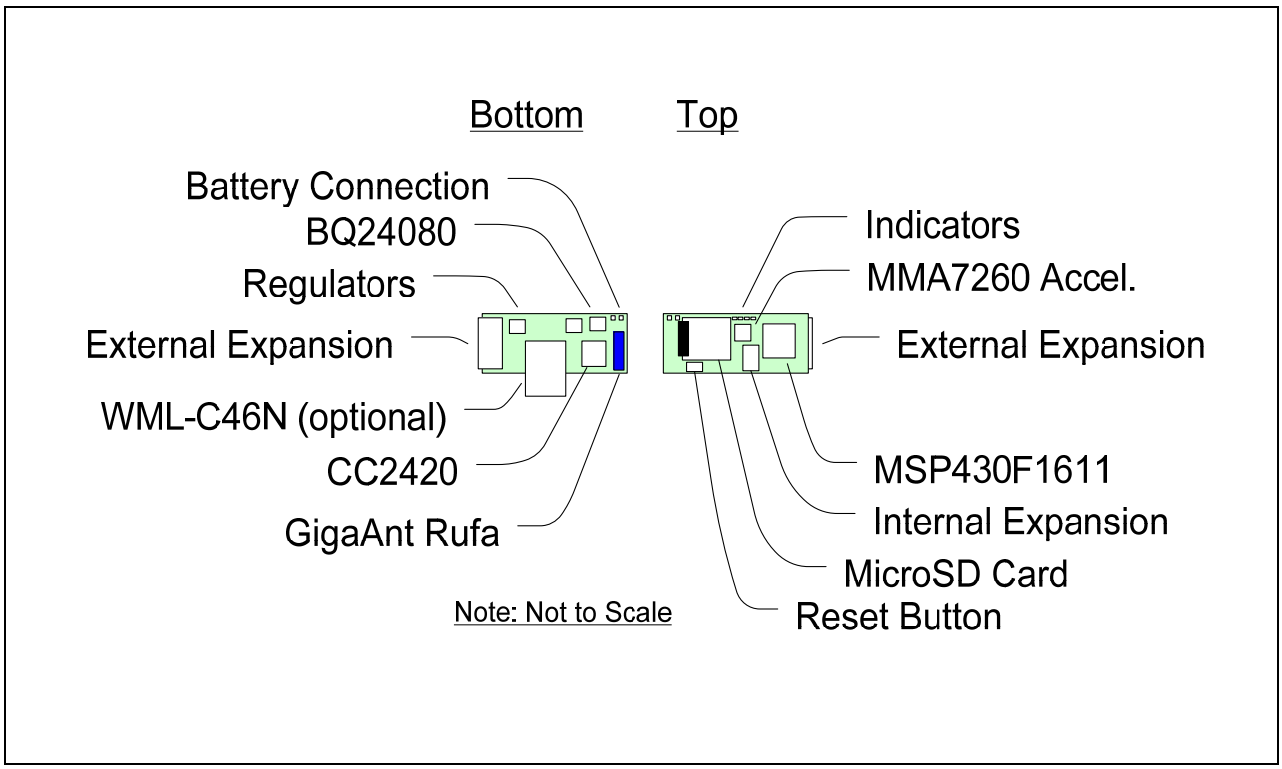
For design validation and testing TinyOS which uses the mspgcc Compiler is recommended. TinyOS offers economy due to the extensive open-source code library for the Telos Mote platform. Retargeting existing Telos applications to SHIMMER is one of the proficiencies of the TinyOS environment and will greatly accelerate design bring-up and validation.

SHIMMER platform code has been released by Intel and is actively maintained at:
http://tinyos.cvs.sourceforge.net/tinyos/tinyos-1.x/
in contrib/handhelds

Current functionality includes:
Flash card operations
Reliable TCP/IP stack for 802.15.4
Telnet server
Http server
Accelerometer control
Real time clock module
LED control
Low voltage alert
Low-power ADC using DMA-mode

A Command Shell is in progress

4 Board Description



Pinout for External Expansion Connector:

Pin	Net Name	Function
1	PV_CHG	Battery Charging Power 5-6.5VDC at 300ma (limited by Internal Expansion connector current rating)
2	SER0_RXD	USART0: Serial
3	SER0_TXD	USART0: Serial
4	SPI0_SCLK_EXP	USART0: SPI
5	SPI0_SOMI	USART0: SPI
6	SPI0_SIMO	USART0: SPI
7	JTAG_MSP_TCK	BSL programming
8	MSP_RESET_N	BSL programming and board reset
9	PV_1P8	Board power output: 1.8VDC
10	GPIO_EXTERNAL	Unspecified GPIO (suggested use is SPI chip select)
11	BSL_RX	BSL programming
12	VSENSE_ADC0	ADC input or GPIO
13	VSENSE_ADC7	ADC input, GPIO or DAC output

14	BSL_TX	BSL Programming
15	SER0_RTS	USART0: Serial
16	SER0_CTS	USART0: Serial
17	PV	Board power output: 3.0VDC
18	GND	Board Ground

Notes:

- BSL_TX/RX can be used as GPIO
- BSL_TX/RX and Serial CTS/RTS can be used as ext. interrupt lines
- I2C is multiplexed onto SPI bus 0 lines.

Pinout for the Internal Expansion Connector. For function description previous table:

Net name	Pin Number	Pin Number	Net Name
PV	1	20	PV_1P8
GND	2	19	GND
SER0_RTS	3	18	SPI0_SIM0
VSENSE_ADC6	4	17	SPI0_SOMI
VSENSE_ADC2	5	16	MSP_RESET_N
VSENSE_ADC1	6	15	JTAG_MSP_TCK
BSL_TX	7	14	SPI0_SCLK_EXP
SER0_CTS	8	13	SER0_TXD
GPIO_INTERNAL	9	12	SER0_RXD
BSL_RX	10	11	PV_CHG

Notes:

- BSL_TX/RX can be used as GPIO BSL_TX/RX and Serial CTS/RTS can be used s ext. interrupt lines
- I2C is multiplexed onto SPI bus 0 lines.

CPU Pin Assignment
TI MSP430F1611

	Pin	Pin #	Name	Use	Type
POWER	DVCC	1	PV_MSP	Power	Analog
	AVCC	64	PV_MSP	Power	Analog
	VREF+	7	PV_VREF_MSP	A/D Ref	Analog
	VeREF+	10	GND	A/D Ref	Analog
	DVSS	63	GND	Power	Analog
	AVSS	62	GND	Power	Analog
	VREF-	11	GND	A/D Ref	Analog
JTAG	TCK	57	JTAG_TCK	BSL	Input
	TMS	56	No Connect	Not Routed	N.C.
	TDI	55	No Connect	Not Routed	N.C.
	TDO	54	No Connect	Not Routed	N.C.
	RST_N	58	MSP_RESET_N	BSL, Button	Open Drain
CLOCK	XIN	8	CLK_MSP_XIN	Primary XTAL	Clocking
	XOUT	9	CLK_MSP_XOUT	Primary XTAL	Clocking

	XT2IN	53	No Connect	Optional XTAL	Clocking
	XT2OUT	52	No Connect	Optional XTAL	Clocking
PORT1	P1.0	12	RADIO_FIFO	802.15.4	Input (IRQ)
	P1.1	13	BSL_TX	BSL	Output
	P1.2	14	RADIO_SFD	802.15.4	Input (IRQ)
	P1.3	15	SER0_RTS	USART0: Serial	Output
	P1.4	16	SER0_CTS	USART0: Serial	Input (IRQ)
	P1.5	17	BT_PIO	Bluetooth	Output
	P1.6	18	BT_RTS	Bluetooth	Output
	P1.7	19	BT_CTS	Bluetooth	Input (IRQ)
PORT2	P2.0	20	GPIO_EXTERNAL	Ext. GPIO or CS (SPI0)	Unassigned
	P2.1	21	GPIO_INTERNAL	Int. GPIO or CS (SPI0)	Unassigned
	P2.2	22	BSL_RX	BSL	Input
	P2.3	23	1WIRE_PWR	802.15.4 MAC	Output
	P2.4	24	1WIRE_DATA	802.15.4 MAC	Bi-directional
	P2.5	25	ROSC	Unused	Pull-up
	P2.6	26	RADIO_FIFOP	802.15.4	Input (IRQ)
	P2.7	27	RADIO_CCA	802.15.4	Input (IRQ)
PORT3	P3.0	28	SPI0_CS_SDFLASH_N	FLASH CS (SPIO0)	Output
	P3.1	29	SPI0_SIMO0	USART0: SPIO0/I2C	Output
	P3.2	30	SPI0_SOMI	USART0: SPIO0	Input
	P3.3	31	SPI0_SCLK	USART0: SPIO0/I2C	Output
	P3.4	32	SER0_TXD	USART0: SERIAL	Output
	P3.5	33	SER0_RXD	USART0: SERIAL	Input
	P3.6	34	BT_TXD	USART1: Bluetooth	Output
	P3.7	35	BT_RXD	USART1: Bluetooth	Input
PORT4	P4.0	36	LED_RD_N	LED	Output
	P4.1	37	LED_OR_N	LED	Output
	P4.2	38	LED_YE_N	LED	Output
	P4.3	39	LED_GR_N	LED	Output
	P4.4	40	ACCEL_SEL0_N	Accelerometer	Output
	P4.5	41	ACCEL_SEL1_N	Accelerometer	Output
	P4.6	42	ACCEL_SLEEP_N	Accelerometer	Output
	P4.7	43	REG_1V8_EN_N	Secondary Regulator	Output
PORT5	P5.0	44	RADIO_SFD	802.15.4	Input
	P5.1	45	SPI1_SIMO	USART1: SPI1	Output
	P5.2	46	SPI1_SOMI	USART1: SPI1	Input
	P5.3	47	SPI1_SCLK	USART1: SPI1	Output
	P5.4	48	SPI1_CS_RADIO_N	802.15.4 CS (SPI1)	Output
	P5.5	49	BT_RESET	Bluetooth	Output
	P5.6	50	NC_RADIO_VREG_EN	802.15.4	N.C.
	P5.7	51	RESET_RADIO_N	802.15.4	Output
PORT6	P6.0	59	VSENSE_ADC0	Ext. GPIO or ADC	Unassigned
	P6.1	60	VSENSE_ADC1	Int. GPIO or ADC	Unassigned
	P6.2	61	VSENSE_ADC2	Int. GPIO or ADC	Unassigned
	P6.3	2	VSENSE_ACCEL_Z	Accelerometer	Analog Input

	P6.4	3	VSENSE_ACCEL_Y	Accelerometer	Analog Input
	P6.5	4	VSENSE_ACCEL_X	Accelerometer	Analog Input
	P6.6	5	VSENSE_ADC6	Int. GPIO, ADC or DAC	Unassigned
	P6.7	6	VSENSE_ADC7	Ext. GPIO, ADC or DAC	Unassigned

4.1 Component detail for debug and testing

These components may be removed or replaced to support specific user applications, configure the board, or perform power-measurement testing:

J1 Negative battery terminal
J2 Positive battery terminal
R25 Primary regulator bypass jumper. Remove U7 when using this option
U7 Primary Regulator (3.0V LDO)
U9 Secondary Regulator (1.8V LDO)
EU6 Battery charger (BQ24080)
R22 Battery charger RSET
X1 32.768 crystal
X2 16.000 MHz crystal for 802.15.4
X3 XT2 clock source (currently 8MHz resonator)
R8 CPU power jumper (use for power measurements or additional filtering)
U2 CPU (MSP430F1611)
U8 Mitsumi WML-C46N footprint
R23 1.8V power jumper (use for power measurements or additional filtering)
EU5 802.15.4 Radio (CC2420)
U4 802.15.4 Antenna (RUFA)
R9 Accelerometer power jumper (use for power measurements or additional filtering)
EU1 3-Axis Accelerometer (MMA7260Q)
R31 Accelerometer x-filter
R29 Accelerometer y-filter
R27 Accelerometer z-filter
C37 Accelerometer x-filter
C36 Accelerometer y-filter
C35 Accelerometer z-filter
J3 MicroSD socket
U3 Unique Silicon Serial ID# (DS2411)
SW1 Reset button
D1 Green LED
D2 Yellow LED
D3 Orange LED
D4 Red LED
J4 Internal Expansion (DF128-20DS-0.5V)
J5 External Expansion (ST80-18P)

4.2 Power

4.2.1 Requirements

Device operating life will depend on application and battery selection however design goal for use as a long-term motion capture device is 1-10 days of operating life from a 250mAh cell while recording 3-axis accelerometer data at 100 samples per second and periodically communicating running status and bursts of data.

The design supports both Lithium-Ion/Lithium-Poly cell chemistry and lithium coin cells or alkaline batteries. Device safety must be maintained by integrating battery polarity protection, charge monitoring and failsafe battery over/under voltage and over-discharge limits in common mobile environments and while AC-powered.

Expansion devices must be current limited according to the following projections:

Case	Primary current	Secondary current	Notes
No Restrictions	25mA	40mA	Sum of internal and external expansion connectors
Bluetooth™ radio in sleep mode	25mA	100mA	60mA secondary current savings is additive in above cases
802.15.4 radio in sleep mode	45mA	40mA	20mA primary current savings is additive in above cases
MicroSD flash memory is idle	50mA	40mA	25mA savings is additive in above cases

Operation beyond these recommended conditions while possible is not recommended without detailed experimental analysis of both electrical and thermal design margin.

4.3 Design Choice

The device uses a diode wired-OR to prevent device damage from reversed battery leads and allow operation from external power while charging. Depending on cell voltages the primary regular can be populated or bypassed during top-level assembly.

The Texas Instruments BQ24080 Smart Li Charger is used for battery management. The BQ24080 implements a multi-phase charge profile including battery conditioning and overcharge protection currently. An Rset (R22) value of 6.49k provides C/2 charge limiting for a 250mAH cell. All battery packs must provide failsafe protection against over/under voltage and over-discharge as a secondary protection.

5 Design Expansions

5.1 Expansion Modules

USB Charger Rev 1.0: Programming board using FTDI UM232 module *(discontinued)*
USB Charger Rev 2.0: Programming board, includes EEPROM, mini-USB type-B connector
GyroDB Rev 1.0: 3-axis Gyroscope + Tilt sensing for kinematics capture
ECG Rev. 1.0: 3-lead Micro-power ECG
AnEx Rev. 1.0: External Connector Breakout board with +/-5VDC Switched Capacitor Regulator

5.2 Recommended pin allocation

To ensure compatibility with existing SW and in cases where both internal and external expansion devices are used, the following conventions are recommended:

External Expansion connector:
Pin 10 (GPIO_EXTERNAL) is pulled low on SHIMMER.
- pull high indicate presence of charging expansion
  - USB Charger 2.0 and higher
- pulse high (button) as USER Attention signal to SHIMMER
  - AnEx Expansion

Pin 14 (BSL_TX) reserved, power-enable/control for internal expansion
Pin 15 (SER0_RTS) power-enable/control for external expansion
- AnEx Expansion – High enables +/-5VDC regulator (recommended SW default: Low)

Pin 16 (SER0_CTS) for 1-wire EEPROM describing expansion
- USB Charger 2.0 and higher

Internal Expansion connector:
Pin 3 (SER0_RTS) reserved, power-enable/control for external expansion
- Used for optional TILYXY_N input on GyroDB

Pin 7 (BSL_TX) power-enable/control for internal expansion
- GyroDB Expansion – Low enables Gyroscopes (recommended SW default: High)

5.3 USB Charger / Programmer

The development charger/programmer is a USB-bus powered cradle using the popular FTDI FT232 UART. Battery Charger status, USB Power, and UART activity indicators are present. There is a reset button and user programmable button.

External Interface, pinout is:

SHIMMER Net name	SHIMMER Pin Number	Expansion Pin Number	Expansion Function
PV_CHG	1	1	PV_CHG (to SHIMMER)
SER0_RXD	2	2	No Connect
SER0_TXD	3	3	No Connect
SPI0_SCLK_EXP	4	4	No Connect
SPI0_SOMI	5	5	No Connect
SPI0_SIMO	6	6	No Connect
JTAG_MSP_TCK	7	7	JTAG_MSP_TCK
MSP_RESET_N	8	8	MSP_RESET_N (optional push button)
PV_1P8	9	9	No Connect
GPIO_EXTERNAL	10	10	GPIO_EXTERNAL (User push button)
BSL_RX	11	11	BSL_RX
VSENSE_ADC0	12	12	No Connect
VSENSE_ADC7	13	13	No Connect

BSL_TX	14	14	BSL_TX
SER0_RTS	15	15	No Connect
SER0_CTS	16	16	EEPROM_IO (not supported on Rev. 1.0)
PV	17	17	PV (from SHIMER)
GND	18	18	GND
GND	SHIELD	SHIELD/MTG pins	GND

5.4 Gyroscope/Tilt Daughterboard

Internal expansion board for motion capture applications. The design uses a pair of InvenSense IDG-300 gyroscopes. The flex segment wraps around the SHIMMER module to properly orient the sensors for X/Y/Z measurement. There is an option to populate binary Tilt detection using Omrom D6B sensors

Internal Interface, pin-out is:

SHIMMER Net name	SHIMMER Pin Number	Expansion Pin Number	Expansion Function
PV	1	20	PV Supply
GND	2	19	GND
SER0_RTS	3	18	TILTXY_N
VSENSE_ADC6	4	17	GYRO_Y
VSENSE_ADC2	5	16	GYRO_Z
VSENSE_ADC1	6	15	GYRO_X
BSL_TX	7	14	GYRO_PWREN_N (Low = Enabled)
SER0_CTS	8	13	TILTZY_N
GPIO_INTERNAL	9	12	No Connect
BSL_RX	10	11	No Connect
PV_VHG	11	10	No Connect
SER0_RXD	12	9	No Connect
SER0_TXD	13	8	No Connect
SPI0_SCLK_EXP	14	7	No Connect
JTAG_MSP_TCK	15	6	No Connect
MSP_RESET_N	16	5	No Connect
SPI0_SOMI	17	4	No Connect
SPI0_SIMO	18	3	No Connect
GND	19	2	GND
PV_1P8	20	1	No Connect

5.5 ECG Daughterboard

Use this internal expansion board for ECG capture. The design uses CMOS operational amplifiers and produces RA->LL and LA->LL vectors. RA->LA can be calculated on the host CPU. Lead inputs have weak pull ups to detect floating electrodes.

Internal Interface, pin-out is:

SHIMMER Net name	SHIMMER Pin	Expansion Pin	Expansion Function

	Number	Number	
PV	1	20	PV Supply
GND	2	19	GND
SER0_RTS	3	18	No Connect
VSENSE_ADC6	4	17	No Connect
VSENSE_ADC2	5	16	ECG_RALL
VSENSE_ADC1	6	15	ECG_LALL
BSL_TX	7	14	No Connect
SER0_CTS	8	13	No Connect
GPIO_INTERNAL	9	12	No Connect
BSL_RX	10	11	No Connect
PV_VHG	11	10	No Connect
SER0_RXD	12	9	No Connect
SER0_TXD	13	8	No Connect
SPI0_SCLK_EXP	14	7	No Connect
JTAG_MSP_TCK	15	6	No Connect
MSP_RESET_N	16	5	No Connect
SPI0_SOMI	17	4	No Connect
SPI0_SIMO	18	3	No Connect
GND	19	2	GND
PV_1P8	20	1	No Connect

5.6 AnEx Daughterboard

AnEx is a simple external breakout board for prototyping and experimentation. Wire-solder vias are provided for most signals and the outputs of a SW controllable +/-5VDC regulator (derived from 3.0V rail).

External Interface, pinout is:

SHIMMER Net name	SHIMMER Pin Number	Expansion Pin Number	Expansion Function
PV_CHG	1	1	No Connect
SER0_RXD	2	2	Wire Via
SER0_TXD	3	3	Wire Via
SPI0_SCLK_EXP	4	4	Wire Via
SPI0_SOMI	5	5	Wire Via
SPI0_SIMO	6	6	Wire Via
JTAG_MSP_TCK	7	7	No Connect
MSP_RESET_N	8	8	Wire Via – RESET
PV_1P8	9	9	No Connect
GPIO_EXTERNAL	10	10	No Connect
BSL_RX	11	11	No Connect
VSENSE_ADC0	12	12	Wire Via
VSENSE_ADC7	13	13	Wire Via
BSL_TX	14	14	No Connect
SER0_RTS	15	15	REG5V_EN (High = Enabled)
SER0_CTS	16	16	Wire Via
PV	17	17	Wire Via – PV
GND	18	18	GND
GND	SHIELD	SHIELD/MTG pins	GND

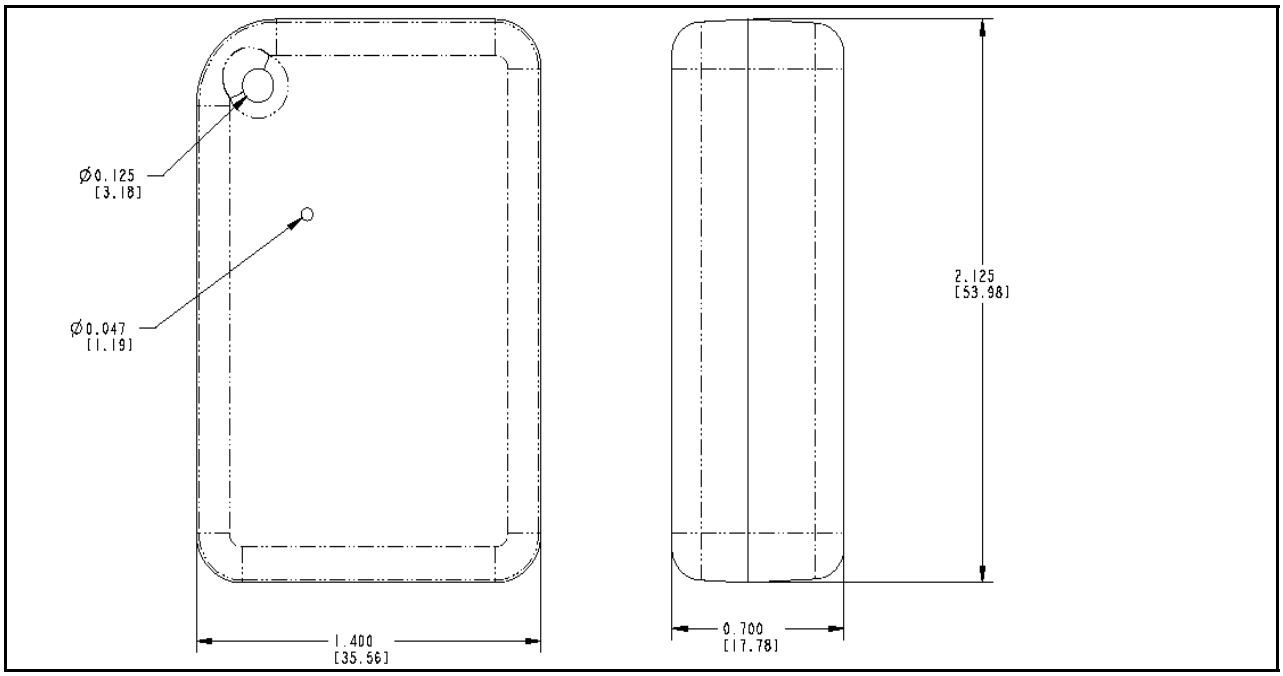
Additional wire vias are provided for:
+5V
-5V
There are also test pads for the unregulated output of the regulator's switching capacitors (~2*PV or 6VDC) located near C14 and C17 respectively.

5.7 Additional Daughterboard Designs

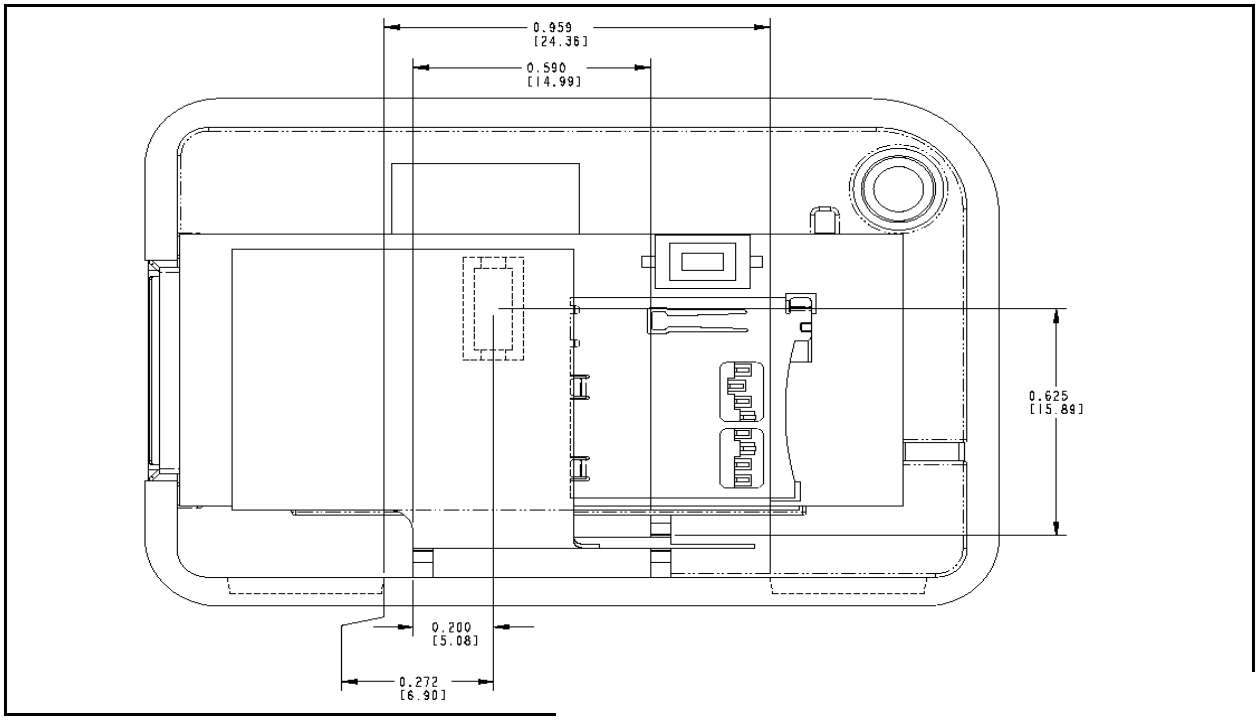
Modular connectors allow for choice of board height. The expansion board dimensions and keep-out area are shown in the attached mechanical drawings. It is recommended to place tall components (2.5mm max with 3.5mm mated connector height) on the SHIMMER side.

6 Mechanical Drawings

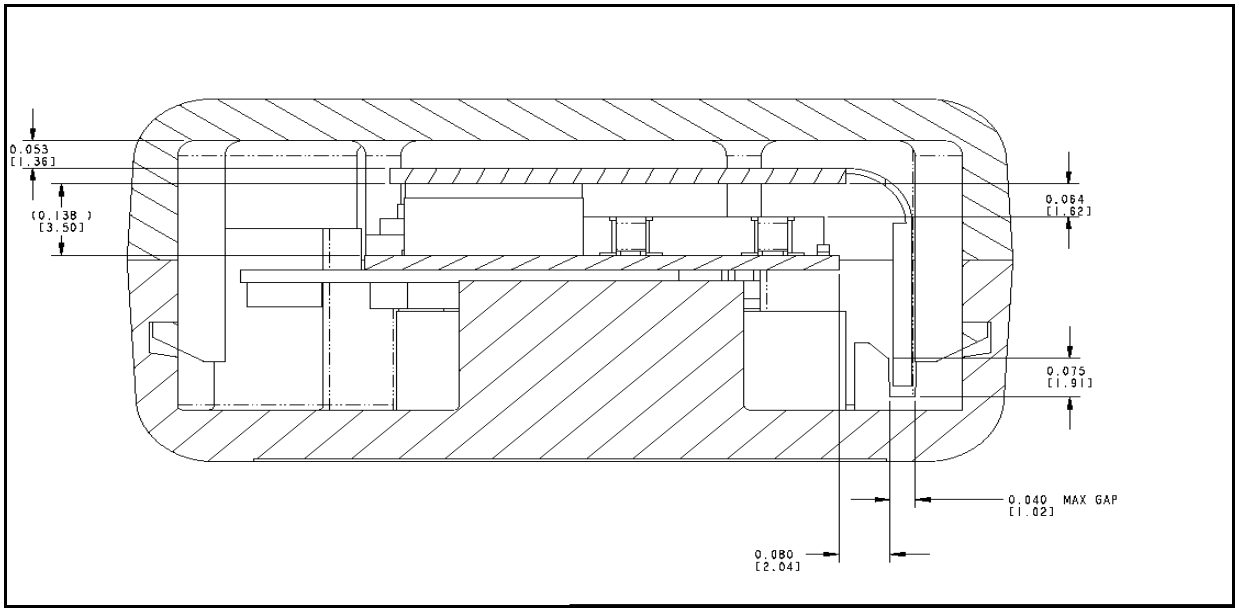
6.1 SHIMMER Enclosure, Outside Dimensions



6.2 SHIMMER Enclosure, Inside Dimensions



GyroDB, Kinematics sensor design is shown from top-view



Component height restrictions including mating dimensions.